

F031 18.846  
09/904,688REMARKS

This amendment is in response to the Examiner's Office Action dated 12/15/2004. As per examiner's suggestion, minor amendments have been made to claims 3, 5, and 10 without adding new matter. Claims 1 and 2 have been amended to clarify applicant's invention without adding new matter. Applicant is appreciative for the recognized allowable subject matter. This amendment should obviate outstanding issues and make the pending claims allowable. Reconsideration of this application is respectfully requested in view of the foregoing amendment and the remarks that follow.

STATUS OF CLAIMS

Claims 1-12 are pending.

Claims 3 and 5 are indicated as containing allowable subject matter.

Claims 1, 2 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiussi et al. (USP 5689505) in view of Timbs (USP 5878585).

Claims 6-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiussi in view of Timbs, and further in view of Roy et al. (USP 6646983).

OVERVIEW OF CLAIMED INVENTION

The presently claimed invention provides a transmission method and apparatus that reduces discarding of data due to delay or overflow in buffers and reduces changes in the transmission order, whereby a meaningless buffer area is avoided and delay of processing is reduced.

The data transmission method of the present invention comprises the steps of:  
controlling switching of connections between a plurality of input ports and an output window

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part having a plurality of buffers in accordance with data storage states of the plurality of buffers; storing data from the plurality of input ports into buffers that have available areas, without detecting a head part of the data, said buffers being included in the plurality of buffers; and multiplexing the data read from the buffers in time division multiplexing for transmission.

The data transmission apparatus of the present invention comprises: an input port part having a plurality of input ports; an output window part having a plurality of buffers; a switch part making connections between the plurality of input ports and the plurality of buffers; a selection control circuit controlling the switch part so that data from the plurality of input ports are stored, without detecting a head part of the data, into buffers that have available areas among the plurality of buffers in accordance with data storage states of the plurality of buffers; and a time division multiplexing part multiplexing the data read from the plurality of buffers in time division multiplexing for transmission.

#### In the Claims

#### CLAIM OBJECTIONS

As mentioned in the preceding 'Remarks' section, as per examiner's suggestion, minor amendments have been made to claims 3, 5, and 10 without adding new matter. Also, claim 2 has been amended to clarify applicant's invention without adding new matter.

#### REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 1, 2 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiussi et al. (USP 5,689,505) in view of Timbs (USP 5,878,585). To be properly rejected under U.S.C. § 103(a), each and every element of the claims must be addressed through known prior art or be recognized as an obvious variation thereof. Applicant contends that the Chiussi and Timbs

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references, either in singularity or in combination, fail to provide for many of the limitations of applicant's claimed invention.

Chiussi et al. teach the multicasting of an ingress cell received at one of a plurality of input ports through a switch network to one or more plurality of output ports. Specifically, Chiussi et al. teach the switching of fixed-length ATM cells (53 bytes), wherein the ATM cells are input to the input ports and stored in cell buffers. After the cells are stored in the cell buffers, the cell information (or the cell head information) is analyzed. As a result of the analysis of the cell information, the routing and arbitration circuit routes the cells to the output ports or paths.

Hence, with regards to claims 1 and 2, applicant contends that the Chiussi reference teaches the reception of an ingress cell including a payload and a output port bitmap segment identifying one or more output ports and means for interpreting the bitmap segment to identify the multistage switch network output ports (see abstract, column 1, lines 53-56 – “the bitmap segment is interpreted to identify output ports” and column 4, lines 23-29). Therefore, applicant concludes that the Chiussi's patent teaches the step (and the implementation of such a step in a system) of analyzing cell information, specifically, cell header information, whereas, both independent claims 1 and 2 of applicant's invention (as clarified via the current amendment) teach the control of switching without detecting a header part of data. Hence, applicant contends that the Chiussi reference fails to disclose or suggest the limitation of “controlling switching of connections between the plurality of input ports and the plurality of buffers, without detecting a head part of the data” in accordance with the data storage information of the plurality of buffers, a requirement of both independent claims 1 and 2.

The patent to Timbs (USP 5,878,045) teaches converting data streams in a cell based communication system. Specifically, Timbs discloses a frame-to-cell converter 413 (see figure 7 of the Timbs reference) used to convert a data transmission stream for transportation in a cell-

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based network 102 (see figure 1 of the Timbs reference). However, Timbs, as specifically cited by the examiner or in its entirety, does not cure the deficiencies of the Chiussi reference as it fails to explicitly or implicitly teach controlling switching without detecting a header part of the data, a claim element of independent claims 1 and 2.

The examiner has rejected claims 6-9 under 35 U.S.C. § 103(a) as being unpatentable over Chiussi in view of Timbs, and further in view of Roy et al. (USP 6,646,983). Dependent claims 6-9 inherit all the limitations of independent claim 2 and the above mentioned arguments for independent claim 2 substantially apply for claims 6-9.

Furthermore, the patent to Roy (USP 6,646,983) merely teaches a network switch that supports TDM, ATM, and variable length packet traffic and includes automatic fault/congestion correction. Specifically, the Roy reference shows, in figure 1, that ATM and IP packets are transported in an SPE of the port processor. However, just as with the Chiussi and Timbs references, the Roy reference does not cure the deficiencies of Chiussi mentioned above as it fails to explicitly or implicitly teach controlling switching without detecting a header part of the data, an element of independent claims 1 and 2.

Accordingly, applicant respectfully contend that the cited documents (i.e., the Chiussi, Timbs, and Roy references) either singularly or in combination fail to anticipate or render obvious the features of the applicant's claimed invention.

#### SUMMARY

As has been detailed above, none of the references, cited or applied, provide for the specific claimed details of applicant's presently claimed invention, nor renders them obvious. It is believed that this case is in condition for allowance and reconsideration thereof and early issuance is respectfully requested.

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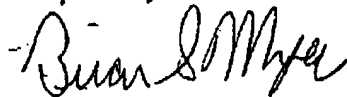
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As has been detailed above, none of the references, cited or applied, provide for the specific claimed details of applicant's presently claimed invention, nor renders them obvious. It is believed that this case is in condition for allowance and reconsideration thereof and early issuance is respectfully requested.

As this amendment has been timely filed within the set period of response, no petition for extension of time or associated fee is required. However, the Commissioner is hereby authorized to charge any deficiencies in the fees provided to Deposit Account No. 50-1290.

If it is felt that an interview would expedite prosecution of this application, please do not hesitate to contact applicant's representative at the below number.

Respectfully submitted,



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